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VEDDER PRICE KAUFMAN & KAMMHOLZ 222 N. LASALLE STREET CHICAGO, IL 60601			HOYE, MICHAEL W	
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			2614	

DATE MAILED: 05/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/398,913

Applicant(s)

KLEBANOV ET AL.

Examiner

Michael W. Hoyer

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 November 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 2-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 2-13, 22 and 23 is/are allowed.
- 6) ☒ Claim(s) 14-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 February 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Response to Arguments

1. Applicants' arguments filed on November 18, 2004, with respect to claims 14-20, have been considered but are moot in view of the new ground(s) of rejection.

Applicants' arguments with respect to claim 14 and the Cheney reference have been fully considered but they are not persuasive.

In response to Applicants' argument that the Cheney reference fails to show certain features of Applicants' invention, it is noted that the feature upon which Applicants rely (i.e., "storing at least a portion of the compressed transport stream data signals, via a first bus, and a memory buffer...") is not recited in the rejected claim. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Applicants' arguments with respect to claim 21 have been fully considered but they are not persuasive.

In response to the Applicants' argument that the same frame buffer store the video data for both modes of operation. The Examiner refers the Applicants to col. 11, lines 34-52 (specifically lines 49-52) of the Schindler reference, where the MPEG data (compressed video) may be provided back to controller 510, which then places the video information into VRAM 518. Moreover, the Schindler reference primarily discloses high-level system components, whereas, the Malladi and Datari references were provided to give additional teaching related to

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the specifics of frame buffer memory storage methods, which one of ordinary skill in the art of frame buffer memory use would look to in order to arrive at the Applicants claimed invention.

Claim Objections

2. Claim 14 is objected to because of the following informalities: There is insufficient antecedent basis for the limitation, “the first bus,” in the last line of the claim. It appears from the Applicants arguments that the previous section of the claim should read, “storing at least a portion of the compressed transport stream data signals, via a first bus, in a memory buffer...” Appropriate correction is required.

Claims 18-20 are objected to because of the following informalities: the claimed “bus interface port” in claim 18, the claimed “interface port” in claim 19, and the claimed “system interface port” in claim 20 seem to be referring to the same port and should be worded as -- **system bus interface port**--. Otherwise as currently claimed, there is insufficient antecedent basis for the limitation, “the interface port”, in line 4 of claim 19 and the limitation, “the system interface port,” in line 2 of claim 20. Furthermore in claim 18, the claimed, “and further includes an engine operative to decompress the compressed transport stream, a graphics engine and a video output port” seems to be repeating the graphics engine twice and should be reworded as -- **and further includes a graphics engine operative to decompress the compressed transport stream, and a video output port**--. In addition to, in claim 19, the claimed “memory interval” does not make sense and seems to be referring to “internal memory” and therefore, should read -- **internal memory**--, also the claimed “transport system port” should be --**transport stream port**--. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheney et al (USPN 6,519,283), in view of So (USPN 5,909,559), both cited by the Examiner.

As to claim 14, note the Cheney et al reference which discloses a method of receiving video graphics data. The claimed "receiving a compressed transport stream associated with a digital video broadcast signal" is met by the digital video from cable or satellite broadcast signal 101 (Fig. 4) received at NIM 102, where a MPEG transport stream is sent to transport logic (XPORT) 103 (see col. 6, line 35-45). The MPEG transport stream is a compressed transport stream. In addition, the claimed "compressed transport stream having data signals and control signals" is inherent to a MPEG transport stream. The Applicants also disclose this in the "Background of the Invention" (or prior art) section of the specification, which describes the Digital Video Broadcast (DVB) transmission standards and specifically states that, "The compressed MPEG 2 format is referred to as a transport stream. The transport stream from the demodulator comprises a plurality of packets. Each of the transport stream packets comprises one synchronization byte, followed by one of 187 data bytes or 187 data bytes plus 16 extra bytes depending on the format." (See Specification, page 1, lines 15-19), in addition to, it is well known in the art that MPEG transport streams may comprise header information with routing

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information. Therefore, it is well known in the art that a MPEG transport stream comprises data signals as met by the data bytes, and control signals as met by the synchronization bytes and header information. The claimed “generating a secondary set of control signals from the compressed transport stream’s control signals” is met by the video decode system of Figure 6, where the MPEG input source is fed through the memory control unit 652 as coded MPEG 2 video data to the input of video decoder 654 and from the decoded signals from the MPEG transport stream’s control signals, the frame buffer pointer control 686 generates additional control signals (see col. 9, line 31 – col. 11, line 46), where a B picture “MPEG-2 repeat field” signal from Huffman decoder 672 of video decoder 654 may be used in part frame buffer pointer control 686 in Fig. 6 (col. 11, lines 5-46). The claimed “storing at least a portion of the compressed transport stream data signals in a memory buffer controlled by the secondary set of control signals” is met by the frame buffer pointer control 686, in one mode, controlling the rotation of the frame buffers as described above (also see col. 10, lines 37-41). Although the Cheney reference discloses a PCI bus 42 (Fig. 2), the Cheney reference does not explicitly disclose the claimed sending the contents of the memory buffer via the first bus to a system bus. The So reference discloses improved integrated circuits and computer system embodiments for desktop and computers, television sets, set-top boxes and appliances improved with asymmetrical multiprocessors (see col. 129, lines 22-37). More specifically, the So reference teaches the use of a multimedia system with multiple buses, including a PCI bus or bus 124 in Fig. 1 (330 in later Figs.), as well as the claimed, “sending the contents of the memory buffer via a first bus to a system bus” as met by the embedded frame buffer 128 sending the contents of the memory buffer via the AGP bus to the AGP port of the north bridge chip 108, where the contents

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may be sent to the PCI or system bus 124/330 through the PCI port (see Figs. 1 and 126-127 and col. 129, line 23 – col. 131, line 30). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have combined the method of receiving video graphics data as disclosed by the Cheney et al reference with the teachings the So reference which discloses using a north bridge integrated interface for multiple buses in conjunction with the frame buffer memory and a system or PCI bus for the advantage of having the ability to receive various types of broadcasts or multimedia streams through a computer system with a video graphics adapter or graphics engine and bus type system. One of ordinary skill in the art would have been led to make such a modification since television/multimedia receivers used with computers are well known in the art to provide additional capabilities within a computer system.

As to claim 15, the Cheney reference discloses multiple modes of operation and a method of receiving a digital video signal that is of a different type than the compressed transport stream, which is met by the video signals received at 104 in Fig. 4 (col. 4, lines 40-42 & 54-57 and col. 6, lines 62-67). The Cheney reference discloses a first mode of operation as shown by receiving a digital video signal 101, which includes a compressed MPEG transport stream (col. 6, lines 37-44). The Cheney reference also discloses another mode of operation wherein the digital video signal is of a different type than the compressed transport stream, which is met by the uncompressed digital video signals received at 104 in Fig. 4 (col. 4, lines 40-42 & 54-57 and col. 6, lines 62-67), which includes data signals including pixel data signals and control signals which are met by the corresponding synchronization signals (col. 4, lines 56-57), and by “pixel select control” signals (col. 7, lines 40-41). The digital multi-standard decoder (DMSD) 105 provides

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synchronization signals, such as, horizontal sync and vertical sync and the DMSD 105 provides the synchronization signals to the video decoder 106 which interprets the synchronization information and processes the data (col. 7, lines 7-18) to provide a secondary set of control signals through the use of the frame buffer pointer control 686 and other circuitry as shown in the video decode system of Fig. 6 and as previously described above in claim 14.

As to claim 16, the Cheney reference as combined above, further discloses a camcorder or television camera may be used as an uncompressed signal and connected video cameras may inherently comprise the transmission of a zoom video signal (see col. 8, lines 24-25 and ZV port definition from the Microsoft Computer Dictionary, p. 586).

As to claim 17, the Cheney et al reference also discloses a method wherein the memory buffer is a frame buffer as shown in Fig. 2, DRAM 53 (col. 5, lines 65-67) and Fig. 6, element 653.

5. Claims 18-20 are also rejected under 35 U.S.C. 103(a) as being unpatentable over Schindler et al (USPN 5,900,867), in view of So (USPN 5,909,559), both cited by the Examiner.

As to claim 18, the Schindler et al reference discloses a system for receiving a digital video broadcast signal. The claimed "tuner to receive a digital broadcast signal and to provide an analog output signal" is met by tuner 410 in Fig. 4, which receives a digital signal (MPEG or MPEG-2) that is transmitted on an analog carrier signal (see col. 10, lines 31-40). The claimed "demodulator coupled to...the tuner, and to provide a transport stream" is met by digital demodulator 412, which demodulates the tuned signal and provides the compressed digital MPEG transport stream signals (col. 10, lines 37-44 and 51-56). The claimed "video graphics

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adapter...” is met in part by the video graphics adapter (VGA) 318, as shown in Fig. 5, where the controller 510 or tuner 526 and/or decoder 530 send the MPEG encoded video stream to the MPEG-2 decoder 512 (col. 11, line 34 – col. 12, line 18). The claimed “video graphics adapter further includes a bus interface port coupleable to a central processing unit” is met by the PCI bus interface port from controller 510 in VGA card 318 (see Fig. 5 and col. 11, lines 35-38), which is coupleable to processor 310 via the PCI Bus (see Fig. 3 and col. 9, lines 17-24). The claimed VGA further includes an engine, or graphics engine, operative to decompress the compressed transport stream is met by the MPEG-2 decoder 512 in Fig. 5, which decompresses the MPEG transport stream (see col. 11, lines 37-44), and the claimed video output port is met by either the audio video output connector 542 (see col. 11, lines 61-63 and col. 12, lines 3-6), or the video output 522 as shown in Fig. 5 (see col. 11, lines 40-55, more specifically lines 52-55). The Schindler et al reference teaches that the digital video broadcast signal as described above is transmitted through the PCI bus 312. Schindler also teaches that the VGA 318 as shown in Fig. 5 may also directly receive broadcast signals through audio and video inputs 524, 544, 546 and 548 (col. 11, lines 56-66), more specifically, standard cable connector 524, which may receive broadcasts, is coupled to tuner circuit 526 (col. 11, lines 56-60). Although the Schindler et al reference does not explicitly disclose that the video broadcast received through connector 524 is a digital video broadcast, and more specifically the claimed, “transport stream port to receive the compressed transport stream and another transport stream”, the So reference teaches improved integrated circuits and computer system embodiments for desktop and computers, television sets, set-top boxes and appliances improved with asymmetrical multiprocessors (see col. 129, lines 22-37). More specifically, the So reference teaches the use of a multimedia system with multiple

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buses, including a PCI bus or bus 124 in Fig. 1 (330 in later Figs.), as well as the claimed, “transport stream port to receive the compressed transport stream and another transport stream” as met by the north bridge chip 108, which has multiple ports and a PCI or system bus connection through the PCI port to the PCI/system bus 124/330 (see Figs. 1 and 126-127 and col. 129, line 23 – col. 131, line 30). Multiple transport streams may be received through the 1394 port and/or TV tuner 130. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have combined the method of receiving video graphics data as disclosed by the Cheney et al reference with the teachings the So reference which discloses using a north bridge integrated interface for multiple buses in conjunction with the frame buffer memory and a system or PCI bus for the advantage of having the ability to receive various types of broadcasts or multimedia streams through a computer system with a video graphics adapter or graphics engine and bus type system, in addition to providing the advantages of reducing hardware components, simplifying the system and bypassing the PCI bus, which would cut manufacturing costs and improve processing speed as shown by the So reference. One of ordinary skill in the art would have been led to make such a modification since television/multimedia receivers used with computers are well known in the art to provide additional capabilities within a computer system and combining the components in to a single system before connecting to the PCI bus as shown by the So reference would provide a more efficient system.

As to claim 19, the Schindler reference discloses a memory to store at least a portion of the compressed transport stream as met by DRAM 514 in Fig. 5 (see col. 11, lines 37-47). The So reference as combined above with Schindler further teaches an internal memory 128 coupled

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to the graphics engine 126, the transport stream port (116 of DSP1), and the system bus interface port (PCI 122) to store at least a portion of the transport stream... as previously described above in claim 14.

As to claim 20, the Schindler reference discloses the claimed central processor unit coupled to the bus interface port of the video graphics adapter as met by processor 310 (see Fig. 3 and col. 9, lines 17-24), which is coupled to the bus interface port (controller 510) of the VGA 318 via the PCI BUS 312 (see Fig. 5 and col. 11, lines 35-38). The claimed transport demultiplexer coupled to the demodulator is met by the demultiplexer 416, which is coupled to the demodulator 412 through the F.E.C. 414 as shown in Fig. 4 (see col. 10, lines 40-58).

6. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schindler et al (USPN 5,900,867), in view of Malladi et al (USPN 5,912,676), and in further view of Datari (USPN 6,418,169), all cited by the Examiner.

As to claim 21, note the Schindler et al reference which discloses a method of storing video data. Schindler et al discloses multiple modes of operation, such as receiving a digital video broadcast signal (MPEG/compressed) from a satellite dish as shown in Fig. 4, or receiving a standard cable broadcast signal at 524 as shown in Fig. 5. The claimed first mode of operation comprising storing pixel information in a frame buffer of a video adapter, wherein one line of frame buffer memory is representative of one line of a video image to be displayed is met in part by receiving an uncompressed signal from a cable video source through connector 524 (Fig. 5), as described above, where the video signal may be buffered in VRAM 518 for output to a monitor (see col. 11, line 56 – col. 12, line 3). Although, Schindler does not explicitly disclose

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that one line of the frame buffer memory is representative of a line of video image to be displayed, it is well known in the art of uncompressed video frame buffers that a line of frame buffer memory may be *representative* of a line of a video image to be displayed. The Malladi et al reference teaches that various frame storage formats exist for storing frame data in memory, and that one method for storing a frame of pixel data is on a scan line basis, where the data is stored in memory scan line by scan line for pictures or frames that are to be displayed (see col. 4, lines 30-37). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the method of the Schindler et al reference which discloses multiple modes of operation and storing video data, with the Malladi et al reference, which specifically teaches that one line of frame buffer memory may be representative of one line of a video image to be displayed for the advantage of providing a storage format which provides improved performance for storing a reference frame of pixel data on a scan line basis. The claimed second mode of operation comprising storing compressed transport stream data in the frame buffer, wherein one line of frame buffer memory is representative of one transport stream packet is met in part by the Schindler et al reference, which also discloses receiving an MPEG transport stream from a digital video source Fig 4, as described above, where the compressed MPEG transport stream is sent to the PCI bus 312, where the video graphics adapter card receives the MPEG stream through controller 510 (Fig. 5, col. 11, lines 34-37), and the MPEG data is routed to MPEG-2 decoder 512 with associated random access memory (DRAM 514), which is used as buffer in assisting with the decoding (see col. 11, lines 37-47) and in lines 34-52 (specifically lines 49-52), the MPEG data (compressed video) may be provided back to controller 510, which then places the video information into VRAM 518 as used by the other

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video signal described above. Although, the Schindler et al reference does not explicitly disclose that one line of the frame buffer memory is representative of one transport stream packet, it is well known in the art of video transport streams that are stored in frame buffers that a MPEG-2 transport stream packet has a fixed 188 byte length as defined by MPEG standards, and therefore, a line of frame buffer memory is *representative* of a transport stream packet since every MPEG-2 transport stream packet has already been produced and transmitted according to the established MPEG standards so that when received by a frame buffer memory a line of memory is representative of one transport stream packet. In addition to, the Datari reference teaches that MPEG video data packets may be stored or buffered in memory and sequentially accessed by priority (see col. 5, lines 13-42 and col. 6, lines 62-66, also see col. 8, lines 10-18). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further combined the method of Schindler et al which discloses multiple modes of operation and storing video data, with the Datari reference, which specifically teaches that a line of the frame buffer memory may be representative of one MPEG or transport stream packet for the advantage of providing a storage format which allows for improved priority accessing of transport stream packets of video images to be displayed.

Allowable Subject Matter

7. Claims 2-13 and 22-23 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

As to claim 22, the prior art, alone or in combination, does not teach or fairly suggest a video graphics system comprising a data storage controller having at least one pair of a plurality of internal control ports to communicate control signals within the data storage controller.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Naiff (USPN 5,982,363 B1) – Discloses a peripheral device for a personal computer that enables the PC to provide the functions of a set-top box for television reception.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael W. Hoyer whose telephone number is (571) 272-7346.

The examiner can normally be reached on Monday to Friday from 8:30 AM to 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller, can be reached at (571) 272-7353.

Any response to this action should be mailed to:

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to customer service whose telephone number is (571) 272-2600.

Michael W. Hoyer
May 13, 2005



JOHN MILLER
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600